(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 047 196 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
25.10.2000 Bulletin 2000/43

(51) Int. Cl.[7]: **H03L 7/089**, H03L 7/183

(21) Application number: **99830234.3**

(22) Date of filing: **21.04.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(71) Applicant:
STMicroelectronics S.r.l.
20041 Agrate Brianza (Milano) (IT)

(72) Inventors:
- **Magazzu', Antonio**
  98124 Messina (IT)
- **Marletta, Benedetto Marco**
  95025 ACI S.Antonio, Catania (IT)
- **Gramegna, Giuseppe**
  95100 Catania (IT)
- **D'Aquila, Alessandro**
  90144 Palermo (IT)

(74) Representative: **Botti, Mario**
Botti & Ferrari S.r.l.
Via Locatelli, 5
20124 Milano (IT)

(54) Method and circuit for minimizing glitches in phase locked loops

(57) The invention relates to a method and a circuit (7) for minimizing glitches in phase-locked loops. The circuit is of the type which comprises an input terminal (EXT) connected to an input of a phase detector (8); a series of a charge pump generator (9), a filter (10) and a voltage controlled oscillator (11) connected downstream of the phase detector (8); and a frequency divider (12) feedback connected between an output of the voltage controlled oscillator and a second input of the phase detector (8).

The invention provides for the inclusion of a compensation circuit (13) connected between the charge pump generator (9) and the filter (10) to absorb an amount of the charge passed therethrough. This compensation circuit (13) includes a storage element (14) connected in series to a switch (15) which is controlled by a control signal (Cpoff) from the charge pump generator (9).

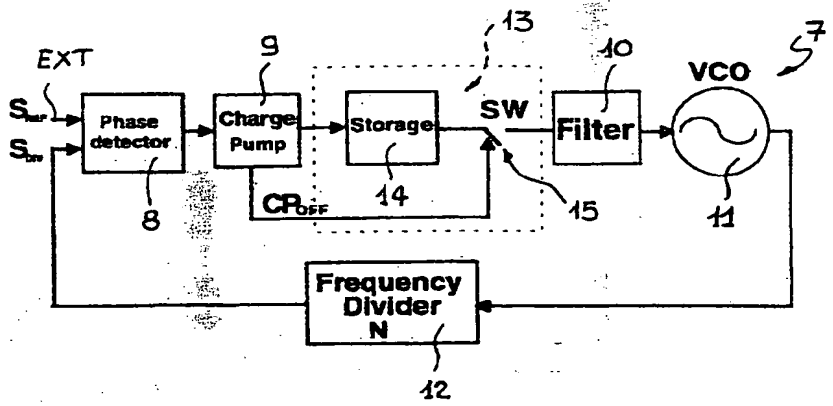


FIG. 7

EP 1 047 196 A1

Description

Field of the Invention

[0001] This invention relates to a method and a circuit for minimizing glitches in phase-locked loops.

[0002] Specifically, the invention relates to a circuit for minimizing glitches in phase-locked loops, of the type which comprises an input terminal connected to an input of a phase detector; a series of a charge pump generator, a filter and a voltage controlled oscillator connected downstream of the phase detector; and a frequency divider feedback connected between an output of the voltage controlled oscillator and a second input of the phase detector.

Prior Art

[0003] As is well known, a PLL (Phase Lock Loop) as generally shown at 1 in Figure 1 comprises essentially a phase comparator 2, a filter 3, a frequency divider 4, and a voltage controlled oscillator VCO 5.

[0004] With the phase lock loop PLL 1 locked to a periodic input signal at a frequency Fref, the frequency Fvco of the voltage controlled oscillator VCO 5 is equal to that of the input signal multiplied by a division ratio N of the frequency divider 4.

[0005] The phase comparator 2 then generates a signal which is proportional to the phase difference between the input signal and the output signal of the frequency divider. This signal modifies, through the filter 3, the control voltage of the voltage controlled oscillator VCO 5, and consequently its frequency Fvco as well, thereby bringing the output frequency Fdiv of the frequency divider 4 to the same value as the input frequency Fref.

[0006] The characteristic parameters according to which a phase lock loop PLL 1 is evaluated are:

- accuracy of the generated frequency;
- phase noise;
- glitch rejection;
- locking time; and
- loop phase margin.

[0007] The frequency accuracy of the voltage controlled oscillator VCO 5 is dependent on the frequency accuracy of the input signal and the accuracy of the phase comparator 2.

[0008] Specifically, it is:

$$\Delta Fvco = N * \Delta Fref + \Delta\Phi/2*\pi * Fvco \qquad (1)$$

where,

$\Delta Fvco$ is the frequency error of the voltage controlled oscillator VCO 5;

N is the division ratio of the frequency divider 4;

$\Delta Fref$ is the frequency error of the input signal;

$\Delta\Phi$ is the phase error of the phase comparator 2; and

Fvco is the output frequency of the voltage controlled oscillator VCO 5.

[0009] System specifications covering certain communication standards provide for the largest frequency error of the voltage controlled oscillator VCO 5 to be in the 10^{-8}*Fvco range. For example, the GSM Standard sets the maximum error to $2*10^{-8}$*Fvco.

[0010] In this case, assuming one half of that frequency error to be due to inaccuracy of the input frequency (usually obtained from a crystal oscillator), the maximum acceptable phase error would be $6*10^{-8}$ radians.

[0011] Such a restricted value for the phase error rules out the use a Gibert cell for a phase comparator, since this cell exhibits a minimum phase error which lies well above said limit. Furthermore, a Gibert cell type of phase comparator would exhibit a non-constant system loop gain in the phase locked range of operation.

[0012] Thus, for standard practical applications, the phase comparator is provided in a charge pump form, using first Icharge and second Idischarge current generators, having the same Icp value and opposite signs, which generators will vary the output control voltage in opposite directions according to whether the output signal of the frequency divider 4 is leading on or lagging behind the input signal. A block diagram for a phase lock loop PLL 1' comprising a charge pump 6, according to the prior art, is shown in Figure 2.

[0013] To avoid phase errors and variations in the loop gain of the phase lock loop PLL 1' near the locking range, a time interval Tmin is usually provided when both current generators, Icharge and Idischarge, deliver equal and opposite currents, such that the input voltage to the filter 3 will remain unchanged, as shown in Figure 3. Thus, the current generators Icharge, Idischarge are turned on at each cycle to ensure that the frequency of the voltage controlled oscillator VCO 5 remains locked to the value N*Fref.

[0014] The use of a filter 3' with two-poles and a zero, as schematically illustrated in Figure 4, is conceivable. This filter 3' comprises a resistive element R1 connected in series to a first capacitive element C1, between a terminal T1 and a voltage reference such as a ground GND. The filter 3' also comprises a second capacitive element C2, connected between said terminal T1 and ground, in parallel with said resistive element R1 and said first capacitive element C1.

[0015] The settling time is dependent on the overall loop gain, its phase margin, the filter size, and the maximum admissible frequency error.

[0016] Using the filter 3', it is readily seen that the proportionality of the settling time Ts is:

$$Ts \propto \frac{N*R1*C1}{Icp*Ko} * \ln\left(\frac{B}{\Delta F\,max}\right)$$

where,

N is the division ratio;

Icp is the charge pump 6 current;

Ko is the oscillator VCO 5 gain;

R1, C1 are elements of the filter 3';

B is the channel jump of the oscillator VCO 5;

ΔFmax is the maximum frequency error of the oscillator VCO 5.

[0017] Formula (2) brings out that to obtain short settling times, as is normally required, in wide band, small frequency error systems, it is necessary to use very high values for the charge pump 6 current and filters having decidedly small time constants.

[0018] Reasonable values for conventional systems of the GSM and DCS types are:

$$Icp = 4mA, \text{ and}$$

$$t = 25\mu s.$$

[0019] Thus, by suitable dimensioning of the filter and the charge pump, a phase lock loop PLL could be provided with a settling time value according to specification. However, such dimensioning would be at variance with the specified rejection of glitches at frequencies that are multiples of the reference frequency Fref of the phase lock loop PLL 1.

[0020] In fact, a real phase look loop PLL 1 would exhibit, as a result of process tolerances, a non-pure frequency spectrum, like that shown in Figure 5.

[0021] In particular, the two most evident glitches locate a distance equal to the reference frequency Fref away from the lock frequency Fvco of the voltage controlled oscillator VCO 5. Other glitches, located farther from the oscillation frequency Fvco, are filtered and reduced to a large extent.

[0022] It should be noted that glitches are mainly due to two different phenomena, namely the leakage current of the VCO control terminal and a dissymmetry between the two generators of the charge pump.

[0023] In particular, the leakage current of the VCO control node is the sum of the leakage currents of the charge pump and the VCO. The contribution from the latter is generally dominant because, at the frequencies of interest, the VCO would essentially consist of an LC resonator, wherein the frequency variation is obtained by varying the voltage across a junction capacitance which has a fairly large leakage current.

[0024] The overall leakage current causes the control voltage of the VCO to change proportionally to that current, even with the VCO in the locked state, during the "off" period of the current generators of the charge pump. Consequently, at each cycle, the charge pump is to balance the amount of charge lost during the "off" period.

[0025] Thus, the control voltage waveform shows a periodic trend with a period 1/Fref, and this periodic signal generates glitches at frequencies that are multiples of the reference frequency Fref. It can be seen, therefore, that the amplitude of such glitches is directly proportional to the leakage current and inversely proportional to the value of the second capacitive element C2 of the filter 3'.

[0026] As a result, in transmission systems designed to strict specifications as to settling time and glitches, this contribution to the overall glitch requires that VCOs with very low associated leakage values be used. There are VCOs commercially available which meet both specifications for conventional transmission systems.

[0027] The generation of glitches is also due to asymmetry of the two generators of the charge pump. Particularly in the locked condition, in order to prevent the frequency of the VCO from varying, the average voltage value at the control node must be kept constant. The amounts of charge supplied by the two current generators must, therefore, be equal and opposite.

[0028] Assuming that in the locked condition one of the generators is delivering a current Icp for a time interval Tmin, and that the current error is ΔIcp between the two generators, advantageously in this invention, the second generator would deliver a current Icp+ΔIcp for a time interval equal to Tmin-ΔTmin, to satisfy the following relation:

$$Icp*Tmin = (Icp+\Delta Icp)*(Tmin-\Delta Tmin) \quad (3)$$

[0029] Illustrated by way of example in Figure 6 are waveforms representing the currents generated by the two current generators of the charge pump, as well as the difference between the two currents, equal to the current Ifiltro at the filter 3 in the locked condition.

[0030] In particular, it should be noted that the total amount of charge supplied to the filter 3 is zero, it being given as the difference of two identical values.

[0031] This current Ifiltro generates a periodic variation in the filter voltage, in turn generating glitches at frequencies that are multiples of the reference frequency Fref. These glitches are directly proportional to

the asymmetry of the current generators, ΔIcp, and the value of the "on" period Tmin of the generators, and are inversely proportional to the filter capacitance C2.

[0032] The contribution to the generation of glitches from the asymmetry of the current generators in applications for which strict settling time specifications are provided, is an order of magnitude larger than the contribution from leakage.

[0033] Therefore, the requirements for settling time values and glitch generation are difficult to meet simultaneously, especially in transmission systems designed to strict specifications. In fact, whereas to obtain limited durations of the settling time a large charge current Icp must be used for the charge pump along with a very small filter capacitance C2, the error percent between the current generators, and the respective turn-on times, should be quite small.

[0034] Conventional circuit designs, and technological limitations setting a minimum turn-on time for a current generator, make meeting the specifications very difficult.

[0035] The underlying technical problem of this invention is to provide a phase lock loop which can minimize the generation of glitches and overcome the limitations of prior art circuits so as to meet, for example, the specifications established for transmission systems.

Summary of the Invention

[0036] The concept behind this invention is one of avoiding direct connection of the charge pumpa to the filter, thereby suppressing the glitch due to asymmetry between the current generators of the phase comparator.

[0037] Based on this concept, the technical problem is solved by a phase lock loop as previously indicated and defined in the characterizing portion of Claim 1.

[0038] The problem is also solved by a method for minimizing the generation of glitches, as previously indicated and defined in the characterizing portion of Claim 9.

[0039] The features and advantages of the device and the method according to the invention will become apparent from the following description of an embodiment thereof, given by way of non-limitative example with reference to the accompanying drawings.

Brief Description of the Drawings

[0040] In the drawings:

Figure 1 shows a phase lock loop according to the prior art;

Figure 2 shows a phase lock loop with a charge pump, according to the prior art;

Figure 3 shows qualitative patterns of internal signals of the phase lock loop of Figure 2;

Figure 4 shows a detail of the phase lock loop of Figure 2;

Figure 5 shows the frequency spectrum of a VCO incorporated to the phase lock loop of Figure 2;

Figure 6 shows qualitative patterns of further internal signals of the phase lock loop of Figure 2;

Figure 7 shows a phase lock loop with a charge pump, according to the invention;

Figure 8 shows a first embodiment of the phase lock loop of Figure 7;

Figure 9 shows a detail of the phase lock loop of Figure 7;

Figure 10 shows qualitative patterns of internal signals of the phase lock loops of Figure 2 and Figure 7;

Figure 11 shows a second embodiment of the phase lock loop of Figure 7.

Detailed Description

[0041] Referring to the drawing views, the numeral 7 generally denotes a phase lock loop with a charge pump embodying this invention, shown in schematic form.

[0042] Similar to the loop 1 described above in connection with the prior art, the loop 7 has a terminal EXT which receives an external reference signal Sref and is connected to the input of a phase detector 8.

[0043] The phase detector 8 is further connected to a series of a charge pump generator 9, a filter 10, and a voltage controlled oscillator VCO 11.

[0044] The oscillator VCO 11 is also fed back to the input of the phase detector 8 through a frequency divider 12.

[0045] Advantageously in this invention, the loop 7 further comprises a compensation circuit 13 connected between the charge pump generator 9 and the filter 10.

[0046] In particular, the compensation circuit 13 comprises a storage element 14 connected in series with a controlled switch 15. The switch 15 is controlled by a control signal Cpoff issuing from the charge pump generator 9.

[0047] The operation of the loop 7 according to the invention will now be described.

[0048] The switch 15 is controlled to open during the power-on of the current generators incorporated to the charge pump generator 9. Thus, in the locked condition and in the presence of dissymmetry between said

current generators, a filter current If will be flowing through the storage element 14, allowing an amount of charge to build up in this element.

[0049] Actually, at the end of the conduction period of the generators inside the charge pump generator 9, the charge built-up in the storage element 14 will be nil, as shown in Figure 6 already discussed in connection with the prior art.

[0050] Thus, the provision of a compensation circuit 13 is effective to suppress the contribution from glitches appearing in the loop 7.

[0051] Advantageously in this invention, the compensation circuit 13, with its mechanism of charge build-up in the storage element 14, will absorb the amount of charge passed through the charge pump generator 9. In this way, any leakages from the generator or charge build-ups due to dissymetries on its inside are accommodated.

[0052] Shown in Figure 8 is a first embodiment of the loop 7 of

[0053] Figure 7. In particular, the storage element 14 comprises essentially a capacitor Cstorage connected between the output of the charge pump generator 9 and a voltage reference, such as a ground GND.

[0054] The capacitor Cstorage should be of limited capacitance not to affect the transfer function of the loop 7 as a whole. This implies a limited capability of the capacitor Cstorage of storing charge.

[0055] In particular, outside the locked condition of the loop 7, the turning on of one of the two current generators in the charge pump generator 9, being proportional to the difference between the reference signal Sref and a feedback signal Sdiv supplied to the input of the phase detector 8 from the frequency divider 12, will generate too large an amount of charge for storing in the capacitor Cstorage.

[0056] To obviate this potential drawback, a modified embodiment of this invention is provided as shown in Figure 8. Adavantageously in this modification, the switch 15 comprises first SW1 and second SW2 elementary switches, connected in parallel with each other between the charge pump generator 9 and the filter 10 and respectively controlled by a signal LOCK from the phase detector 8 and a signal Cpoff from the charge pump generator 9.

[0057] In particular, the first elementary switch SW1, controlled by the signal LOCK, closes when the loop 7 is not in a locked condition and opens when the phase difference between the signals Sref and Sdiv is smaller than a predetermined threshold value. The second elementary switch SW2, controlled by the signal Cpoff, opens before the turning on of the charge pump generator 9 and closes after this is turned off.

[0058] The switches and capacitors can be integrated simultaneously by current techniques. There remains to be integrated the filter 10.

[0059] The phase lock loop 7 of this invention will, therefore, have the same number of pins and non-integratable components as a conventional loop.

[0060] In addition, the pair of elementary switches, SW1 and SW2, are effective to retain the low resistance specifications outside the locked condition, by the switch SW1 having a small equivalent resistance and reduced capacitance in the other conditions, and the switch SW2 comprising small-size transistors, in particular smaller than those used in switch SW1.

[0061] It should be noted that, in practicing the invention, the parasitic capacitances associated with the elementary switches SW1 and SW2 will cause charge to pass between the capacitor Cstorage and the filter even in the locked condition and absence of a leakage current, specifically upon the elementary switches changing of state.

[0062] This passage of charge through the second elementary switch SW2 generates glitches, because of its disturbing effect on the state of the control node of the oscillator VCO 11.

[0063] The passage of charge through the first elementary switch SW1 produces a variation in the control voltage of the oscillator VCO 11, which may result in a shift of the locked condition.

[0064] Accordingly, it will be expedient to minimize this charge passage inside the elementary switches SW1 and SW2 by designing them for compensation of charge upon changeover.

[0065] A possible circuit embodiment of a compensated elementary switch 16 is shown in Figure 9.

[0066] The switch 16 has an input terminal IN, an output terminal OUT, and a control terminal CONTROL. In particular, the control terminal of the first elementary switch SW1 receives the signal LOCK, and the control terminal of the second elementary switch SW2 receives the signal Cpoff, their respective input terminals being connected to the charge pump generator 9 and their respective output terminals being connected to the filter 10.

[0067] The switch 16 includes a pass-gate PG1 which is connected between the input terminal IN and the output terminal OUT and consists of a first NMOS transistor M1 and a second PMOS transistor M3 whose control terminals are coupled to the control terminal CONTROL.

[0068] In particular, the control terminal of the first transistor M1 is connected to the control terminal CONTROL through a first inverter INV1, and the control terminal of the second transistor M3 is connected to the control terminal CONTROL through a series of second INV2 and third INV3 inverters. Thus, the transistors M1 and M3 of the pass-gate PG1 are driven in phase opposition, thereby ensuring compatibility of the switch 16 input with connection to both a ground reference and a supply terminal.

[0069] The switch 16 further comprises first M2a and second M2b PMOS compensation transistors having their source and drain terminals shorted together and connected to the input IN and output OUT terminals

of the switch 16. The compensation transistors M2a and M2b also have their control terminals connected together and to the control terminal CONTROL of the switch 16 through the series of the inverters INV2 and INV3.

[0070] The transistors M2a and M2b are thus driven in phase opposition to the transistor M1.

[0071] Finally, the switch 16 comprises third M4a and fourth M4b NMOS compensation transistors which have their source and drain terminals shorted together and connected to the common source and drain terminals of the transistors M2a and M2b and to the input IN and output OUT terminals of the switch 16, respectively. Furthermore, the compensation transistors M4a and M4b have their control terminals connected together and to the input terminal IN of the switch 16 through the inverter INV1.

[0072] Similar as the transistors M2a and M2b, the transistors M4a and M4b are driven in phase opposition to the transistor M3.

[0073] Advantageously in this invention, the size of the compensation transistors is chosen equal to one half the size of the transistors of the pass-gate PG1.

[0074] How this choice reflects in advantageous features of the inventive device will now be explained.

[0075] In the locked condition, the voltage at the input terminal IN is approximately equal to the voltage at the output terminal OUT. The gate-drain and gate-source capacitances of the first transistor M1 are, therefore, identical.

[0076] With the transistor arrangement of this invention, the compensation transistors M2a and M2b have the same gate-source and gate-drain voltages as the first transistor M1 of the pass-gate PG1. The paralleled gate-source and gate-drain capacitances of these compensation transistors with halved dimensions are equal to the corresponding capacitances of transistor M1.

[0077] In this condition, as the control terminal CONTROL changes its state, the gate nodes of the transistors M2a and M2b move in opposite directions to the gate node of the transistor M1, and the amount of charge injected thereby into the terminals IN and OUT is equal and opposite to the amount of charge injected by the gate-source and gate-drain capacitances of transistor M1.

[0078] The compensation of transistor M3 by transistors M4a and M4b is effected in a like manner.

[0079] By using a filter as described in relation to Figure 9, a disturbance can be obtained which is by a few orders of magnitude less than the disturbance produced by the generator dissymmetry within the charge pump generator.

[0080] Figure 10 shows comparative graphs illustrating the improved performance brough about by the phase lock loop of this invention compared with a prior art loop.

[0081] In particular, Figure 10(a) shows the evolution of current inside the charge pump generator; Figure 10(b) shows the evolution of current in a prior art loop; and Figure 10(c) shows the evolution of current inside the filter in a loop according to the invention.

[0082] It can be seen that the amount of charge injected into the filter upon the switch in the loop of this invention opening and closing is 100 times less than in prior solutions.

[0083] An additional advantage of the phase compensation loop according to the invention is that the glitches originated by the leakage current of the charge pump generator 9 are halved.

[0084] In applications where glitches are to be specially small, prior art arrangements were obliged to use VCOs with minimal leakage currents, as previously pointed out. In this condition, the leakage current of the VCO takes the same order of magnitude as the leakage current of the charge pump generator, thereby playing an important role as regards compliance with design specifications.

[0085] The phase compensation loop of this invention allows the contribution from the leakage current of the charge pump generator to be cut down by one half through a modification of its operating principle. Particularly in the loop of this invention, the second elementary switch SW2 is controlled to open with a half-period delay from its close, thereby halving the filter voltage discharge due to the leakage current of the charge pump generator.

[0086] This modification can be acquired to the operating principle of the charge pump generator by using a flip-flop 17 of the set/reset type connected to a control terminal of said generator, as shown schematically in Figure 11.

[0087] In particular, the flip-flop 17 would be set by the turn-off signal of both internal generators of the charge pump generator 9, and reset by the trailing edge of the reference signal Sref.

[0088] It should be considered that, to arrive at the embodiment shown in Figure 11, the phase detector 8 has been assumed to compare the signals at the raising edges, and the duty cycle of the reference signal Sref assumed to be 50%.

Claims

1. A circuit (7) for minimizing glitches in phase-locked loops, of the type which comprises an input terminal (EXT) connected to an input of a phase detector (8); a series of a charge pump generator (9), a filter (10) and a voltage controlled oscillator (11) connected downstream of the phase detector (8); and a frequency divider (12) feedback connected between an output of the voltage controlled oscillator and a second input of the phase detector (8); characterized in that it comprises a compensation circuit (13) connected between the charge pump generator (9) and the filter (10) to absorb an

amount of the charge passed therethrough.

2. A circuit according to Claim 1, characterized in that said compensation circuit (13) comprises a storage element (14) connected in series to a switch (15) controlled by a control signal (Cpoff) from the charge pump generator (9).

3. A circuit according to Claim 1, characterized in that said switch (15) is open during the turn-on phase of current generators incorporated to the charge pump generator (9).

4. A circuit according to Claim 1, characterized in that said storage element (14) comprises essentially a capacitor (Cstorage) connected between the output of the charge pump generator (9) and a voltage reference (GND).

5. A circuit according to Claim 1, characterized in that said switch (15) comprises first (SW1) and second (SW2) elementary switches connected in parallel together between the charge pump generator (9) and the filter (10).

6. A circuit according to Claim 5, characterized in that said first (SW1) and second (SW2) elementary switches are controlled by a signal (LOCK) from the phase detector (8) and a signal (Cpoff) from the charge pump generator (9), respectively.

7. A circuit according to Claim 6, characterized in that said first elementary switch (SW1) is closed while the loop circuit (7) is in a non-locked phase condition.

8. A circuit according to Claim 5, characterized in that each elementary switch is a compensated type and has an input terminal (IN), an output terminal (OUT), and a control terminal (CONTROL), and that a pass-gate (PG1) is connected between the input terminal (IN) and the output terminal (OUT) and comprises a first NMOS transistor (M1) and a second PMOS transistor (M3) having respective control terminals coupled to the control terminal (CONTROL), a first pair of compensation transistors (M2a,M2b) driven in phase opposition to the first NMOS transistor, and a second pair of compensation transistors (M4a,M4b) driven in phase opposition to the second PMOS transistor.

9. A method for minimizing the generation of glitches in phase lock circuits, comprising a series of:

a phase detector (8);

a charge pump generator (9);

a filter (10) and a voltage controlled oscillator (11);

and comprising a frequency divider (12) feedback connected between an output of the voltage controlled oscillator and an input of the phase detector (8);

characterized by a compensation circuit (13) being connected between the charge pump generator (9) and the filter (10) to absorb an amount of the charge passed therethrough.

10. A method according to Claim 9, characterized in that said compensation circuit (13) includes a storage element (14) connected in series to a switch (15) controlled by a control signal (Cpoff) from the charge pump generator (9).

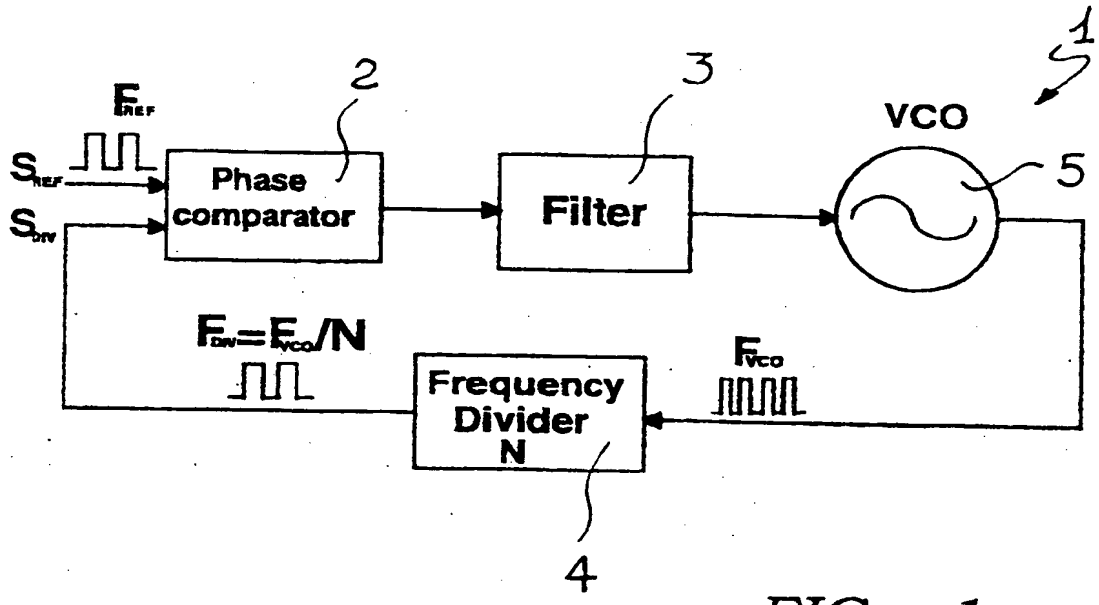


FIG. 1
PRIOR ART

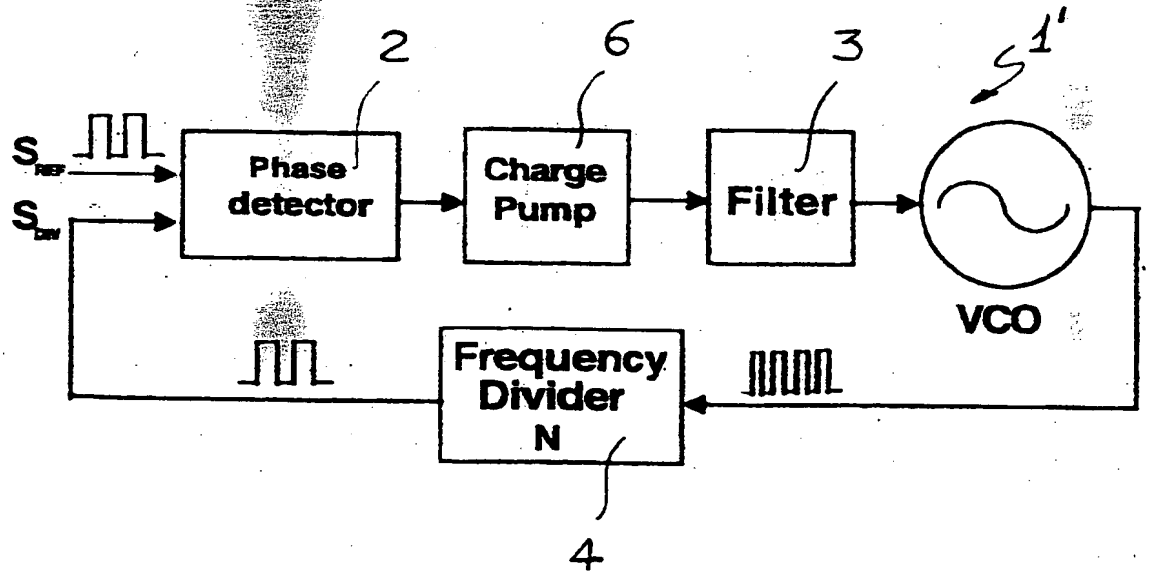


FIG. 2
PRIOR ART

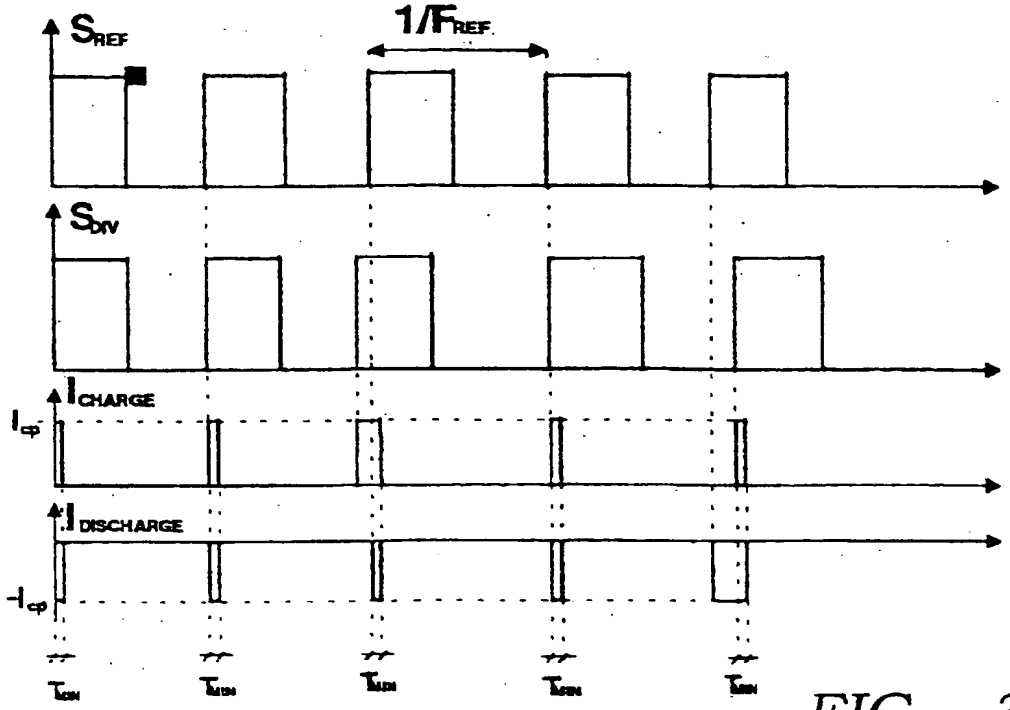


FIG. 3
PRIOR ART

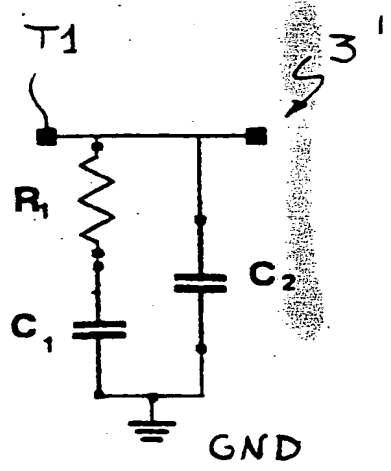


FIG. 4
PRIOR ART

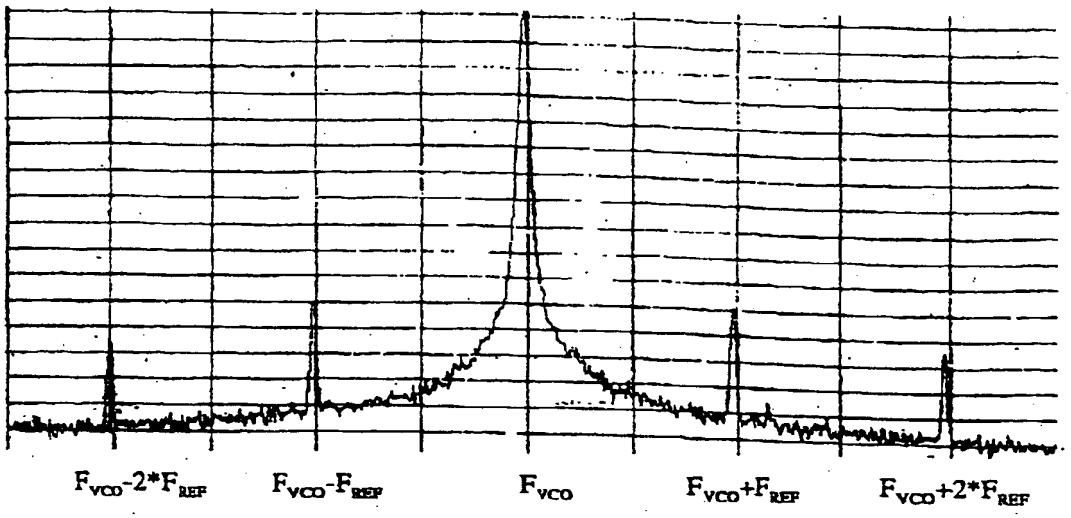


FIG. 5
PRIOR ART

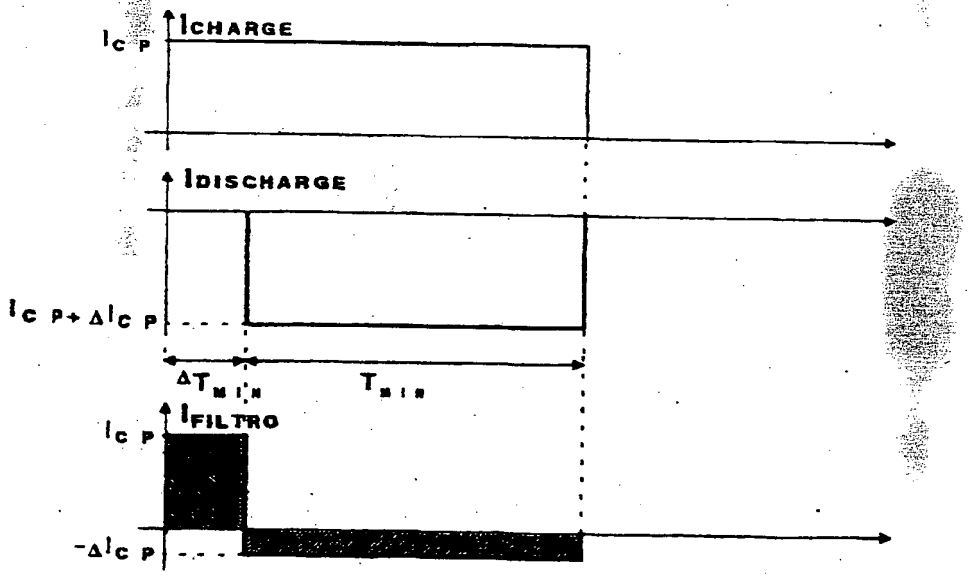


FIG. 6
PRIOR ART

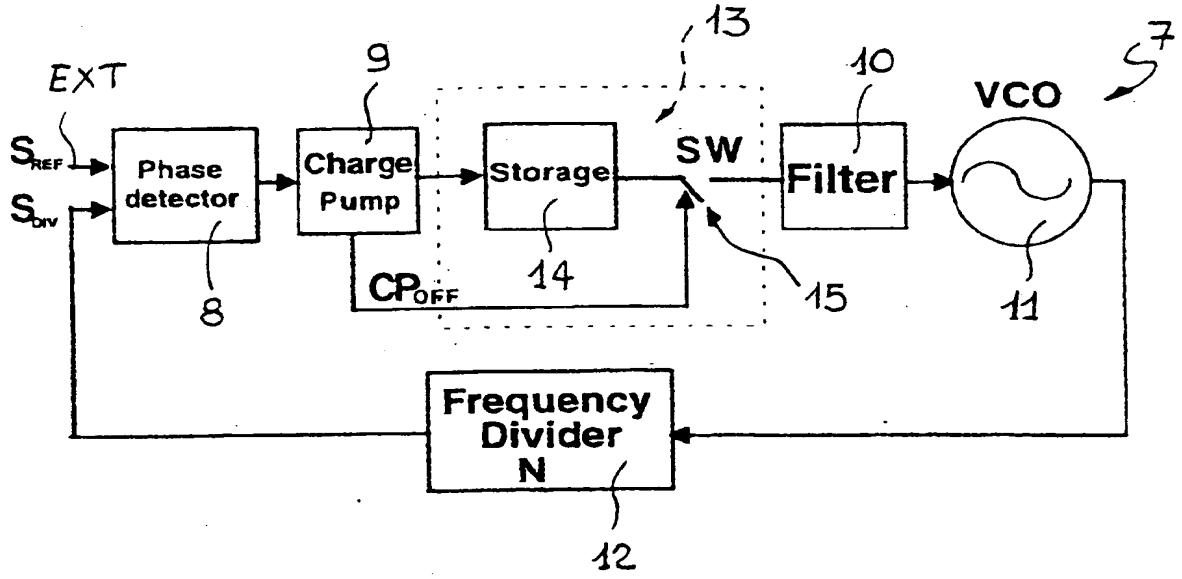


FIG. 7

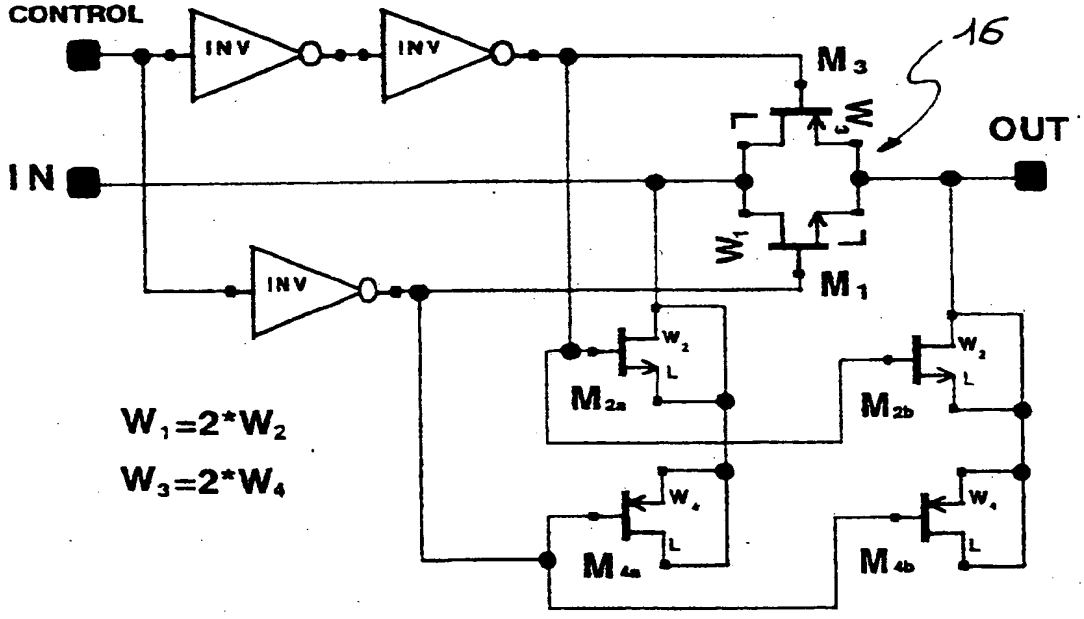


FIG. 9

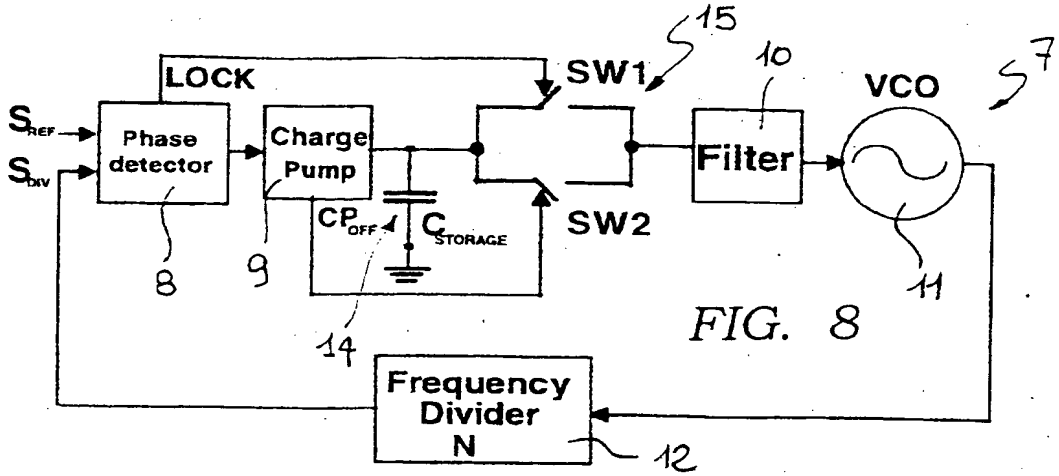


FIG. 8

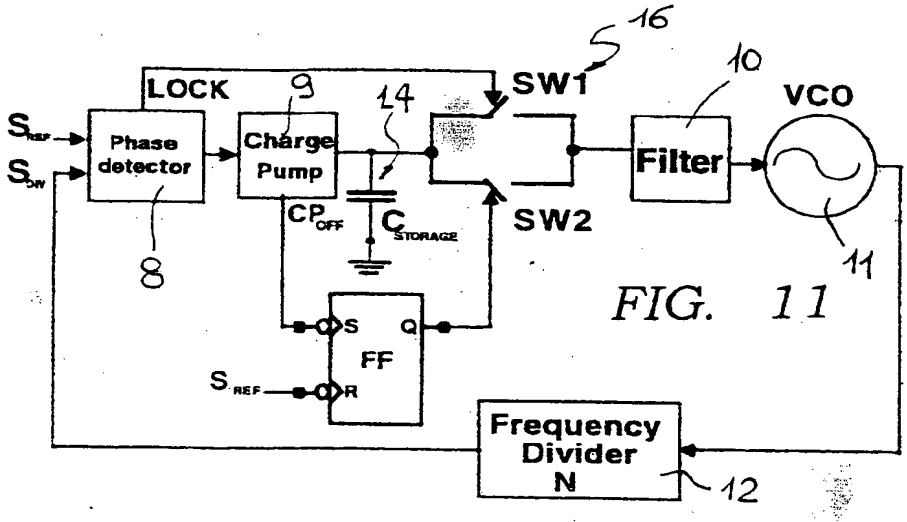
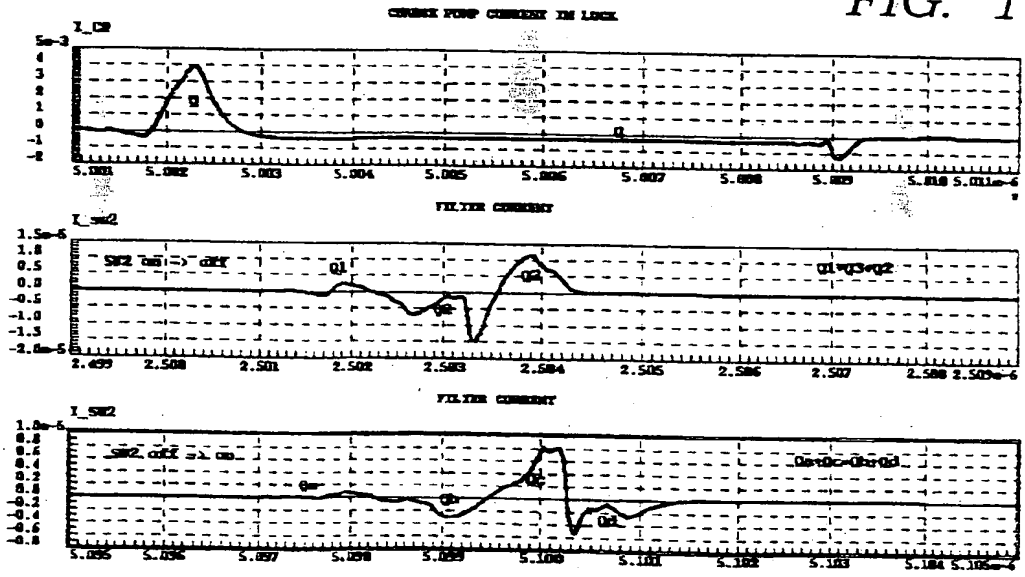


FIG. 11

FIG. 10



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 83 0234

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	WO 98 23035 A (PEREGRINE SEMICONDUCTOR CORP) 28 May 1998 (1998-05-28) * page 10, line 11 - page 17, line 3; figures 3,4,5A-5D *	1-7,9,10	H03L7/089 H03L7/183
Y		8	

Y	US 4 988 902 A (DINGWALL ANDREW G F) 29 January 1991 (1991-01-29) * column 3, line 43 - column 4, line 37 * * column 7, line 52 - column 11, line 44; figures 7-9 *	8	

Y	US 4 651 037 A (OGASAWARA KAZUO ET AL) 17 March 1987 (1987-03-17) * column 1, line 12 - line 57 * * column 6, line 34 - line 65; figures 10-12 *	8	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H03L
H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	21 September 1999	Balbinot, H

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 83 0234

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

21-09-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9823035 A	28-05-1998	US 5920233 A	06-07-1999
US 4988902 A	29-01-1991	NONE	
US 4651037 A	17-03-1987	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82